Remarks

Reconsideration of this application is requested. Claims 1, 3, 5, 15, 17, 18, 19 and 21 have been amended. Claims 16 and 20 have been withdrawn and claims 1-15, 17-19 and 21-22 remain in the application.

Specification

In the Office action the disclosure was objected to for the informality on page 4, lines 6-7, that describes coupling to mean that two or more elements are in direct physical or electrical contact. By this amendment the line in question has been removed from the specification.

Response to the 35 U.S.C. §112 Rejection

The Office Action states that claims 3 and 5 are rejected under 35 U.S.C. 112, fourth paragraph, for failing to further limit the independent claims. In particular, independent claim 1 is a method claim and dependent claims 3 and 5 are directed to structural elements. Claims 3 and 5 have been redrafted, placing the claims in a form having method limitations.

Response to the 35 U.S.C. §103(a) Rejection

The Office Action rejects claims 1-2, 4, 6-11, 15 and 18-21 under 35 U.S.C. 103(a) as being unpatentable over Maloney et al. (US 5,907,464) and in view of Hirayama et al. (US 5,461,338).

Rejection of claims 1-2 and 4

Applicants' claim 1 recites a method for reducing the leakage current through a charge protection device in an integrated circuit. The method includes reverse body biasing junction diodes formed by source and drain regions in a bulk region of the charge protection device when the integrated circuit is in operation.

The Examiner states that Maloney et al. teach a PFET 502 transistor in FIG. 5 that is used as an ESD clamp to conduct charge away during an ESD event, yet the transistor is turned off during normal operating conditions. The PFET 502 transistor

is a P-channel transistor built in an N-type well, with the well shown connected to the source. This connection provides both a well and a source having a common bias, namely a voltage potential of V_{CC}. But note that in the structure shown, the PN junction formed by the well and the source of PFET 502 has a zero bias across that diode junction. This embodiment for PFET 502 having a commonly connected well and source cannot provide a reverse body biasing; only zero biasing across the diode. Therefore, this embodiment does not teach or suggest Applicants' base claim 1 that calls for reverse body biasing the charge protection device.

The Examiner further relies on the embodiment disclosed in FIG. 10 and states that PFET 1024 and NFET 1026 control the substrate biasing to PFET 1010. Applicants respectfully disagree, pointing out that transistors 1024 and 1026 only provide a gate drive to PFET 1016 and do not affect, nor provide, a reverse body biasing to PFET 1016. Applicants point out that it is PFET 1016 that both sets and generates the body biasing for PFET 1010. In the embodiment illustrated in FIG. 10, a positive potential is supplied at node 1005 and a negative potential, or ground, is supplied at node 1003. It is respectfully pointed out that the voltage potential generated by PFET 1016 must have a value between those supplied from nodes 1005 and 1003. It is not possible for the voltage potential generated by PFET 1016 and supplied to the bulk region of PFET 1010 to reverse bias both of the junction diodes formed by the source and drain regions with the bulk region. Accordingly, Maloney et al. does not teach or suggest at least this feature of Applicants' claim 1. Rejected claims 2 and 4 depend directly from base claim 1 and are believed allowable for at least the same reasons as Applicants' claim 1.

The relied upon reference of Hirayama et al. teach detecting a normal operation mode and a standby mode of an IC. The bias potential from the substrate region to the source region of the transistor is altered to change the threshold voltage of the transistor based on a detected mode of operation. Hirayama et al. teach reducing power consumption by raising the threshold voltage of transistors during a standby mode.

Further, in column 2, lines 26-39, Hirayama et al. teach applying a reverse bias to the substrate in a standby mode. Whereas Hirayama et al. teach applying a reverse bias to a transistor in a standby mode, i.e., a non-operating mode, Applicants' claim 1 includes reverse body biasing junction diodes formed by source and drain regions in a bulk region of the charge protection device when the

integrated circuit is in operation. Since, Hirayama et al. do not teach or suggest at least this feature of Applicants' claim 1 the relied upon reference cannot make obvious Applicants' claim. Rejected claims 2 and 4 depend directly from base claim 1 and are believed allowable for at least the same reasons as Applicants' claim 1.

It is well established that obviousness requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Without conceding the appropriateness of the combination, Applicants respectfully submit that the combination of Maloney et al. and Hirayama et al. does not meet the requirements of an obvious rejection in that neither teach nor suggest reverse body biasing junction diodes formed by source and drain regions in a bulk region of a charge protection device.

Applicants would like to emphasize that the preceding paragraphs were not intended to attack Maloney et al. and Hirayama et al. separately. But instead, Applicants have shown how each is devoid of claimed elements so that, by default, the combination is also devoid of at least some of the features of Applicants' claimed invention.

Rejection of claims 6-11

Applicants' FIG. 1 illustrates an embodiment for a charge protection device that includes a resistive element 30 that may be used to reverse bias a charge protection device 50. Applicants' claim 6 recites, among other things, a charge protection device coupled to an integrated circuit and a resistive element adapted to reverse bias the charge protection device.

On the other hand, Maloney et al. in column 9, lines 23-26, teach a long-channel resistive PFET 1020 to charge a capacitor 1012, with the RC timer setting a time to shut off conduction of ESD protection device 1010. But whereas Maloney et al. teach a resistive element and capacitive element connected to the gate of protection device 1010, Applicants' claim 6 includes a resistive element adapted to reverse bias the charge protection device. This feature of Applicants' claim 6 is not taught or suggested by Maloney et al.

Hirayama et al. does not teach or suggest using a resistive element to affect a reverse bias of the charge protection device. Since neither Maloney et al. nor Hirayama et al. teach or suggest a resistive element adapted to reverse bias a charge protection device, Applicants believe that the art of record cannot make

obvious Applicants' claimed invention. Claims 7-11 depend, either directly or indirectly, from independent claim 6 and are believed to be allowable for at least the same reasons as Applicants' claim 6.

Rejection of claims 15

The Office Action states that claims 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim. The element and features in Applicants' dependent claim 16 have been incorporated into base claim 15. It is believed that base claim 15 and dependent claim 17 are now allowable.

Rejection of claims 18-21

Applicants' claim 18 recites a first transistor coupled between a positive power conductor and a ground power conductor to provide charge protection for an integrated circuit, and a resistive element coupled to provide a bulk region of the first transistor with a voltage potential that is greater than a voltage potential supplied on the positive power conductor.

Support for the amended claim language can be found at least in FIG. 1 where a first transistor, i.e., transistor 50, is coupled between a positive power conductor V_{CC} and a ground power conductor. A resistive element, i.e., element 30, is coupled to provide a bulk region of the first transistor with a voltage potential V_{CCP} that is greater than a voltage potential V_{CC} supplied on the positive power conductor.

Since neither Maloney et al. nor Hirayama et al. teach or suggest a voltage potential that is greater than a voltage potential supplied on the positive power conductor, these references cannot anticipate or make obvious Applicants' claim 18. Claims 19, 21 and 22 depend from base claim 18 and are believed allowable for at least the same reasons as Applicants' base claim 18.

Allowed Claims

Applicants would also like to gratefully acknowledge the Examiner's indication that claims 12-14, 16-17 and 22 would be allowable if the objection as being dependent upon a rejected base claim were overcome. The subject matter of claim

16 has been incorporated into claim 15. Other base claims are believed to be allowable over the art of record.

Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed December 2, 2003, and it is submitted that claims 1-15, 17-19 and 21-22 are in condition for allowance. Reconsideration of the rejection of claims is requested and the allowance of amended claims is earnestly solicited.

Should it be determined that a fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 552-1388 is respectfully solicited.

Respectfully submitted,
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